CALL FOR GRANT APPLICATIONS
(AE2024-0517)

INESC TEC is now accepting grant applications to award 1 Research Grant (BI) within the A-IQ Ready project with reference 101096658, funding from the European Key Digital Technologies Joint Undertaking partnership, under the Horizon Europe programme, and by National Funds through FCT - Foundation for Science and Technology, I.P.

1. GRANT DESCRIPTION

Type of grant: Research Grant (BI)

General scientific area: ENGINEERING

Scientific subarea: Electrical engineering

Area of Work: Informatics, Electronics and Digital Systems, Digital Electronics, Microprocessors, Heterogeneous Systems

Grant duration: 11 months 17 days, starting on 2025-01-15.

Scientific advisor: Nuno Miguel Paulino

Workplace: INESC TEC, Porto, Portugal

Maintenance stipend: € 990,98, according to the table of monthly maintenance stipend for FCT grants , paid via bank transfer. Grant holders may be awarded potential supplements, according to a quarterly evaluation process (Articles 19, 21 and 22 of the Regulations for Grants of INESC TEC and Annex II), up to a maximum limit of 50% of the monthly maintenance stipend.

INESC TEC supports costs with registration, enrolment or tuition fees, during the grant duration, under the terms established in the internal document: "Payment of Tuition fees to grant holders".

The grant holder will benefit from health insurance, supported by INESC TEC.

2. OBJECTIVES:

- Continue the implementation of a RISC-V core based on C/C++ code, for use in simulation, and implementation in hardware via High-Level-Synthesis (HLS) techniques.
- Designing and testing an SoC that integrates the RISC-V processor as the main processor.
- Writing a co-authored scientific article to disseminate the results obtained.

3. BRIEF PRESENTATION OF THE WORK PROGRAMME AND TRAINING:

- Familiarization with open-source implementations of RISC-V processor-based SoCs.
- Familiarization with the existing C/C++-based RISC-V processor codebase, and identification of value-added contributions.
- Expansion of the existing core with additional features, mainly an in-house extension for communication with an external accelerator, but also, e.g., instruction extensions for the AI domain or others, or interfaces for communication with accelerators external to the core.
- Encapsulate the core as an IP block, to build the SoC via connection to other IP blocks (e.g. buses, memories, UART etc).
- Validating the SoC by running basic test programs.
- Collaboration in writing a scientific article to disseminate the results.

4. REQUIRED PROFILE:

Admission requirements:

Graduation or enrollment in a master's degree in electrical engineering, computer science, or a related field;
The awarding of the fellowship is dependent on the applicants' enrolment in study cycle or non-award courses of Higher Education Institutions.

Preference factors:

- RISC-V experience;
- experience with Xilinx Vivado/Vitis tools;
- fluent in Portuguese and English (written and spoken).

Minimum requirements:

- experience in HDL and FPGAs;
- fluent in English (written and spoken).

5. EVALUATION OF APPLICATIONS AND SELECTION PROCESS:

Selection criteria and corresponding valuation: the first phase comprises the Academic Evaluation (AC), based on the criteria referred to in Article 12 of the Regulations for Grants of INESC TEC, while the second phase comprehends the Individual Interview (EI). All factors are evaluated on a scale of 0 to 100, taking into account the applicants' merit, suitability and conformity with the preference factors.
The weight of the AC factors are as follows: Academic Qualifications (FA, 40%), Scientific Publications (PC, 10%), Experience (EX, 40%) and Motivation Letter (CM, 10%).
Candidates who score less than 50 points in the AC average will be considered excluded on absolute merit. The top five candidates approved on absolute merit will be qualified for the individual interview. The Final Grade (CF) is obtained by the weighted average of AC (70%) and EI (30%).

DISABILITY INCENTIVE

Candidates who present a degree of disability equal to or greater than 90% will benefit from an incentive (20) in the score of the CV Assessment.
Candidates who present a degree of disability equal to or greater than 60% and less than 90% will also benefit from an incentive (10) in the score of the CV Assessment.
Said score may, in these cases, exceed 100 points.
Candidates must demonstrate the degree of disability during the application, namely through the submission of the Multi-Purpose Medical Certificate of Disability, issued in accordance with Decree-Law no. 202/96, of October 23 - currently in effect.
Candidates must declare, in the application form, the type of disability used throughout the selection process, in order to proceed with the required adaptations.

The Selection Jury is composed of the following members:

President of the Jury: Nuno Miguel Paulino
Full member: João Bispo
Full member: João Canas Ferreira
Substitute member: Vítor Grade Tavares

Release of results and prior hearing: the results of the selection process, as well as the terms and procedures for prior hearing, will be released to the applicants by email, under the terms referred to in Article 13 of the Regulations for Studentships and Fellowships of INESC TEC.

6. FORMALISATION OF APPLICATIONS:

Application Documents:

1. Motivation letter;
2. Curriculum Vitae (must include the list of previous fellowships, their type, beginning and end dates, funding entities and host institutions);
3. Certificate or diploma degree;

4. Proof of enrollment in a degree awarding study cycle or in a non degree awarding Higher Education program.
    - The proof of enrollment may be presented just during the grant hiring stage.
5. Signed declaration stating the infringement of the grant holder's duties (article 14, no. 4)
6. Documental evidence to support the country of residence, residence permit or other legally equivalent document, in cases where the applicant is a foreigner or non-resident in Portugal - valid until the beginning of the grant.
7. Other supporting documents relevant to the final assessment.

Failure to deliver the required documents within the 90-day period after the date of the notice of the conditional awarding of the grant implies its cancellation.

Application period: From 2024-12-06 to 2024-12-19

Submission of applications: the application will be formalised by submitting the form available in the *Work With Us* section of INESC TEC website.

7. BINDING LEGISLATION AND REGULATION

The hiring process shall comply with the current legislation regarding the Research Grant Holder Statute, approved by Law no. 40/2004 of August 18, in its current wording, as well as by the Regulations for Grants of INESC TEC and for FCT Grants Regulation in force.

For more information, please check the Regulations for Grants of INESC TEC and relevant annexes at www.inesctec.pt/bolsas

Funded by the European Union